ECE/CS 757: Advanced Computer Architecture II Midterm 2 Review

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Lecture notes based on slides created by John Shen, Mark Hill, David Wood, Guri Sohi, and Jim Smith, Natalie Enright Jerger, and probably others

Midterm 2 Review

- Transaction Memory (Lect 8)
- Interconnection networks (Lect 9)
  - Topology
  - Routing
  - Flow Control
  - Router Microarchitecture
- SIMD (Lect 10)
- Massively Parallel Processors (Lect 11)
- Clusters (Lect 12)
- GPGPUs (Lect 13)

Transactional Memory

- Transactional programming model
- Hardware Implementation
- Virtual TM (brief)
- Hardware-assisted Software Transactional Memory (brief)
- Thread-level speculation (TLS)

TM Readings

[16] T. Harris, J. Larus, and R. Rajwar, “Transactional Memory, 2nd edition,” Chapter 1 & Chapter 5, Synthesis Lectures on Computer Architecture, http://www.morganclaypool.com/doi/abs/10.2200/S00272ED1V01Y201006CAC011

[17] Harold W. Cain, Maged M. Michael, Brad Frey, Cathy May, Derek Williams, and Hung Le. Robust architectural support for transactional memory in the power architecture. In Proceedings of the 40th Annual International Symposium on Computer Architecture (ISCA '13), June 2013.

Interconnection Networks

- Introduction to Networks
- Network Topologies
- Network Routing
- Network Flow Control
- Router Microarchitecture

Interconnect Readings

- Read: [18] N. Enright Jerger, L.-S. Pei, “On-Chip Networks,” Synthesis Lectures on Computer Architecture, http://www.morganclaypool.com/doi/abs/10.2200/S00209ED1V01Y200907CAC008
- Review: [19] D. Wentzlaff, P. Griffin, H. Hoffmann, L. Bao, B. Edwards, C. Ramey, M. Mattina, C.-C. Miao, J. F. B. III, and A. Agarwal. On-Chip Interconnection Architecture of the Tile Processor. IEEE Micro, vol. 27, no. 5, pp. 15-31, 2007

SIMD & MPP Topics

- SIMD introduction
- Automatic Parallelization for SIMD machines
- Vector Architectures
  - Cray-1 case study

- MPP Introduction
- Software Scaling
- Hardware Scaling
- Case studies
  - Cray T3D & T3E

SIMD & MPP Readings

Read: [20] C. Hughes, "Single-Instruction Multiple-Data Execution," Synthesis Lectures on Computer Architecture, http://www.morganclaypool.com/doi/abs/10.2200/S00647ED1V01Y201505CAC032

Review: [21] Steven L. Scott, Synchronization and Communication in the T3E Multiprocessor, Proceedings of International Conference on Architectural Support for Programming Languages and Operating Systems, pages 26-36, October 1996.

Clusters

- Introduction & Examples
- Case studies
  - VAX Cluster
  - Google Cluster
  - IBM Blade Center
  - Microsoft Catapult
- **Reading:** L. Barroso, J. Clidaras, U. Hölzle, Chapters 1-3, Chapter 5, "The Datacenter as a Computer: An Introduction to the Design of Warehouse-Scale Machines, Second edition," Synthesis Lectures on Computer Architecture, http://www.morganclaypool.com/doi/abs/10.2200/S00516ED2V01Y201306CAC024

GPGPUs

- General Purpose Graphics Processing Unit (GPGPU)
- Programming model overview (SPMD, BSP)
- Hardware features (SIMT)
- Programming environment

- Reading: Chapter 1 of: H. Kim, R. Vuduc, S. Bahsorkhi, J. Choi, W.-M. Hwu, Chapter 1, "Performance Analysis and Tuning for General Purpose Graphics Processing Units (GPGPU)," Synthesis Lectures on Computer Architecture, http://www.morganclaypool.com/doi/abs/10.2200/S00451ED1V01Y201209CAC020

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